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硼掺杂直拉硅单晶 p/p^+ 外延片中铜沉淀的
研究

Investigation of copper precipitation in heavily boron- doped
Czochralski silicon p/p^+ epitaxial wafers

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摘要

半导体材料作为集成电路的基础，地位十分重要。重掺杂硅单晶的应用范围广，性质优良。但是重掺硼硅片不能通过传统的热处理得到洁净区（DZ），但是外延片的结构就可以弥补这一缺点，获得洁净区。门锁效应和软失效是微电子工业中常见的问题，利用外延结构就可方便快捷地解决这一难题。铜具有非常优良的导电性，在集成电路中，如果使用铜就会大大提高其运算速度，并且提高散热效率，但是也会给硅片带来铜污染的危险，然而对铜沉淀在外延片中的形成机理的研究有待进一步深入。所以对重掺硼单晶硅 p/p^+ 外延片来说，很有必要探究铜在其中的沉淀行为，此类研究的学术价值以及工业价值均较高。本文借助腐蚀法和光学显微镜等测试设备，得出如下一些结论：

（1）研究了快速热处理对铜沉淀的影响及在洁净区生成时起的作用。研究发现，样品经过快速热处理及常规退火后，外延层中没有沉淀生成，在样品中形成了洁净区。未经快速热处理处理而只经过常规热处理的样品，洁净区宽度较小，因此可以推断，快速热处理对形成洁净区有很大的帮助，另外研究还发现，洁净区宽度与铜沉淀的引入温度有关，即间隙铜原子的平衡浓度极大地影响了铜沉淀形成中的热力学及动力学过程。

（2）研究了重掺硼 p/p^+ 外延片中点缺陷与氧沉淀相互作用，和不同类型点缺陷和氧沉淀对铜沉淀影响的机理。研究认为，在氧气气氛下热处理时，氧沉淀生成受阻， p^+ 基底中生成的氧沉淀较少，而在氩气和氮气气氛下热处理时，氧沉淀得到促进，最终在 p^+ 基底中的沉淀密度较大。另外，在样品中，有洁净区形成。研究发现，当氧气中热处理，热氧化产生的自间隙硅原子（ Si_i ）会抑制沉淀及缺陷的形成，而在氩气和氮气中热处理时，产生的空位有利于沉淀的形成。最后，可以得出结论：点缺陷的类型可以极大地影响基底中的沉淀密度；以重掺硼硅单晶作为基底的外延结构可以很好地去掉硅片中的铜沾污。

关键词： p/p^+ 外延片；铜沉淀；点缺陷

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Abstract

With the improvement of the microelectronic industry, the requirement for Si materials applied in Ultra Large Scale Integrated Circuit (ULSI) is improving seriously. The heavily boron-doped Czochralski silicon (HB CZ Si) wafers are generally applied to fabricate devices. Denude zone (DZ) was hardly formed in HB CZ Si wafers by means of RTP. Thus, p/p^+ Si epitaxial wafer is an alternative structure to gain a defect free zone just below the surface. Furthermore, p/p^+ epitaxial wafer is an efficient method to solve Softerror and Latch up caused by α particle. Recently, copper wire is generally applied in semiconductor technology, as a result, copper is more easily contaminated the devices. However, few studies were reported about the gettering ability of copper in p/p^+ Si epitaxial wafers, thus, it is very necessary to know the copper precipitation mechanism in p/p^+ Si epitaxial wafers. In this paper, combining with the preferential etching and optical microscopy, some conclusions are acquired and listed below:

(1) The effect of rapid thermal processing (RTP) on the formation of copper precipitation in p/p^+ silicon (Si) epitaxial wafers was systematically investigated. It was revealed that, the bulk microdefects (BMDs) were found only inside the p^+ substrate, manifesting no defects generated in the epitaxial layer. However, it was found that the width of denude zone (DZ) in samples only subjected to L-H two-step annealing was narrower than that of epitaxial layer, It can be concluded that RTP was beneficial to the formation of DZ. Additionally, it was found that the width of DZ has a sharp dependence on the introducing temperature of copper contamination, that is, the corresponding equilibrium concentration of interstitial copper in the Si influences the thermodynamics and kinetics process of the formation of copper precipitation significantly.

(2) The effect of point defects on copper precipitation in heavily boron-doped Czochralski silicon epitaxial wafer has been systematically investigated. It was found that RTP in O_2 ambient would lead to a low density of copper

precipitation in the p^+ substrate, however, high density of copper precipitation was observed in samples that subjected to RTP in Ar or N_2 ambient. Additionally, in all of the samples, no defects were found in the epitaxial layer. On the basis of the experiments, it is found that interstitial silicon will prevent the process of copper precipitation while vacancy has an opposite effect. Furthermore, p/p^+ epitaxial structure could absorb copper impurities that made the epitaxial layer defect free.

Key words: p/p^+ Si epitaxial wafer; copper precipitation; point defects

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